Comparative Study of DC-Link Capacitor Banks Using Physics-Of-Failure Approach

A Thesis Submitted
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Master of Technology

by

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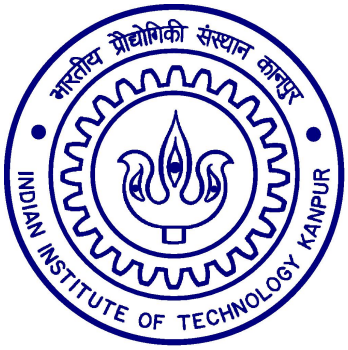

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Statement of Thesis Preparation

1. Thesis title: **Comparative Study of DC-Link Capacitor Banks Using Physics-Of-Failure Approach**

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3. Thesis Guide was referred to for preparing the thesis.

4. Specifications regarding thesis format have been closely followed.

5. The contents of the thesis have been organized based on the guidelines.

6. The thesis has been prepared without resorting to plagiarism.

7. All sources used have been cited appropriately.

8. The thesis has not been submitted elsewhere for a degree.

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Abstract

Due to the flexibility in the control of power electronic converters (PECs), they are routinely used to interface energy sources and electrical loads with different characteristics. These PECs consist of semiconductor switches and passive elements such as inductors and capacitors. Capacitors are used to minimize voltage ripple in the dc-link and to balance the power difference between output load and input source. These banks, typically consisting of Aluminum Electrolytic Capacitors (AEC), are prone to early failure due to various stresses. With time, the electrical parameters of the individual capacitors degrade. Prolonged usage of the capacitor bank will lead to increase in the electrical stress, thereby leading to malfunction of the converter.

Existing literature focuses on reliability improvement of single capacitors in the dc-link rather than a capacitor bank. This work uses a Physics-of-Failure based approach to assess the reliability of a capacitor bank. The method incorporates the circuit, thermal and degradation models in an integrated way to find the time to failure of the bank. With the given constraints, different capacitor bank configurations are simulated and the most reliable capacitor bank is found. Monte Carlo analysis is used to estimate the mean time to failure of specific capacitor banks. A grid connected solar PV inverter is chosen for simulation studies. Monte-Carlo simulations are used to account for variations in the physical parameters of the system. The analysis is validated on a laboratory prototype. The capacitor banks are aged using a combination of accelerated life testing methods. The experimental results are in close agreement with the simulation results.

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Chapter 1

Introduction

Power electronic converters use capacitors to balance the difference between the input power and output power. These capacitors minimize voltage variation in the dc link. In some applications, they are also used to provide sufficient energy during the hold-up time. Typical examples of such applications are shown in Figure 1.1. These Power Electronic Converter(PEC) configurations are used in various industries such as avionics, power drives, wind generation, Photovoltaic (PV) systems,etc. Traditionally single capacitors/capacitor banks are used to fulfill the energy buffer requirement in dc-links.

1.1 Motivation

1.1.1 Reliability of Capacitors

The PECs primarily consist of semiconductor switches and passive elements such as inductors and capacitors. In literature, the survey of field failures of PECs shows that capacitors and semiconductor switches are most prone to failure leading to unscheduled maintenance and thereby increased operational expenses. For example, in grid-connected solar PV inverters, the failure distribution among various components show that capacitors are most prone to failure along with semiconductor switches [1] as shown in Figure 1.2

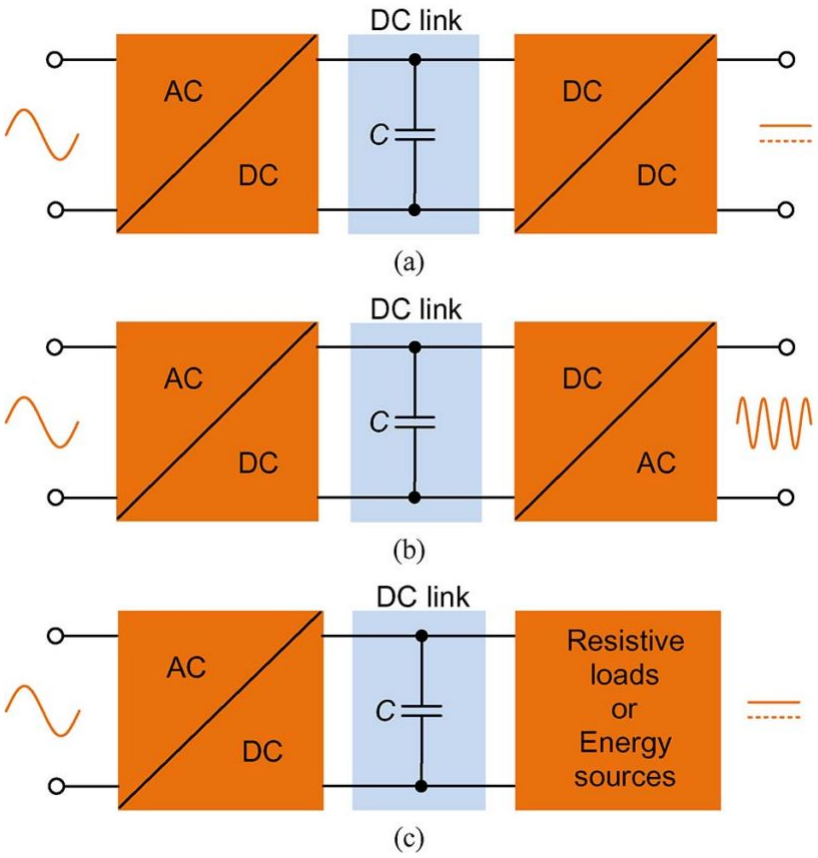

Figure 1.1: Capacitor Configurations in Power Electronic Converters

The commonly used technologies of capacitors are Aluminium Electrolytic capacitors, Multi-Layer Ceramic Capacitors (MLCC) and Metallized Polypropylene Film Capacitors (MPPF). Of these, AECs are predominantly used as they have the least cost and highest energy density. However, the AECs have relatively lower current rating and wear out faster. The failure of AEC can be attributed to the following mechanisms

1. Self-Healing Dielectric breakdown
2. Disconnection of terminals
3. Dielectric breakdown of oxide layer
4. Electrolyte vaporisation
5. Other electrochemical reactions such as anode foil capacitance drop, degradation of the oxide layer.

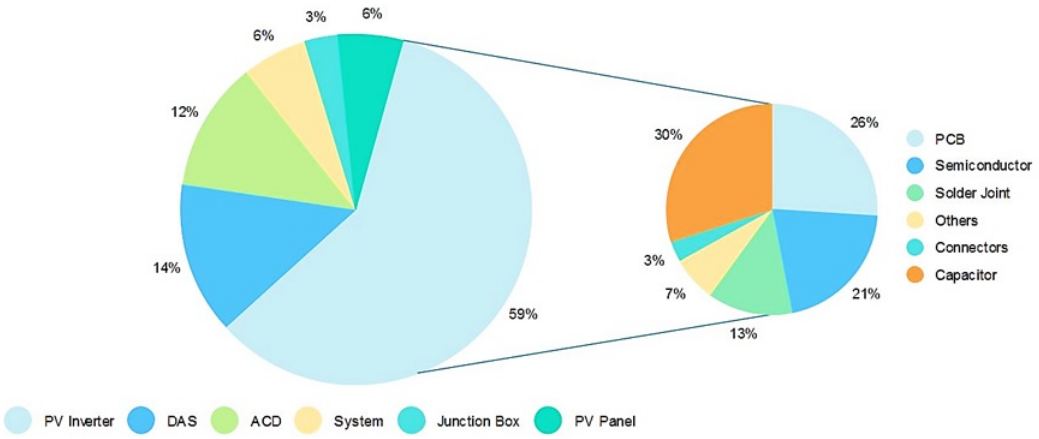

Figure 1.2: Distribution of failure of power component.

Of these methods, the dominant wear out mechanism is the vaporization of the electrolyte. Wear out leads to change in the electrical parameters such as capacitance and Equivalent Series Resistance(ESR). With degradation, C decreases whereas ESR increases [2]. The degraded capacitor loses its power decoupling and filtering capacity which leads to increased voltage ripple in the dc-link. Also, the degradation rate accelerates in a deteriorated capacitor.

1.1.2 Design of Capacitor banks

In practice, capacitor banks are chosen for applications where it is not feasible to use a single capacitor of the desired capacitance, voltage rating and ripple current capability. To match the application requirements, capacitors are connected in series to increase the overall voltage rating and multiple parallel strings of capacitors increase the overall ripple current capability of the bank[3]. However, there is little systematic research on choosing the configuration of the capacitor bank.

1.2 Thesis Outline

The thesis report is divided into the following:

Chapter 2: A detailed literature survey of existing reliability improvement techniques is presented in this chapter

Chapter 3: Modelling of the Aluminum electrolytic capacitor (AEC) used for simulation studies is presented

Chapter 4: In this chapter, the proposed scheme for reliability analysis of dc-link capacitor banks is presented. Simulation studies and results are also discussed

Chapter 5: The proposed analysis is validated on an experimental prototype of a single phase grid connected PV inverter. Detailed description of the hardware along with results is presented

Chapter 6: Conclusion and future scope of the thesis ARE presented in this chapter

Chapter 2

Literature Review

This chapter reviews the existing literature on reliability improvement of dc-link capacitors. The research efforts to solve this problem can be divided into three categories: a) advance the capacitor technology with improved and pre-determined reliability built in, b) optimal dc-link design solutions based on the existing capacitors to achieve proper robustness margin and cost-effectiveness, and c) implementation of condition monitoring to ensure reliable field operation and preventive maintenance. From a Power electronics' perspective, the latter two categories are more relevant and are discussed in this chapter

2.1 Condition Monitoring of Capacitors

There exist multiple methods for condition monitoring of capacitors used in dc-dc converters and inverters. A brief summary of these methods is given here. The methods can be classified into (i) Offline techniques, (ii) Online techniques, and (iii) Quasi-Online techniques. These methods estimate the Capacitance and/or ESR of the AEC and use it as an indicator of health. In online techniques proposed in [4, 5], the current through the capacitor is measured using a current sensor. The RMS value of the current along with average power loss is used to calculate ESR. Invasive methods discussed in [6, 7, 8] involve injection of sub-harmonic current ripple from the source side into the capacitor. Using the capacitor voltage and

reconstructed capacitor current, Capacitance or ESR is estimated using a recursive least squares method. Quasi-online method proposed in [9] modulates the inverter to inject dc-current before starting of the motor. In [10], Power Extraction Efficiency (PEE) is utilized to assess the health of the inverter. It discusses replacement of the capacitor based on PEE to maximize the financial gains from the PV system in a fixed time period. Though there exists much literature on condition monitoring techniques of capacitors, they are complex, involve high cost and thus are rarely used in industrial applications [11].

2.2 DC-link Design Methods

The methods can be categorized into two broad categories, a) Reduction of dc-link capacitance requirement, b) Design of capacitor bank

2.2.1 Reduction of dc-link Capacitance requirement

These methods use clever circuit modifications and strategies to reduce the energy storage requirement in the dc-link so that AECs could be replaced by MPPF-Caps to achieve higher level of reliability without considerable increase in cost and volume.

In [12] a technique is proposed for a single-phase to single-phase full-bridge converter to reduce the AC power in the dc-link and thereby the capacitance required to maintain the same voltage ripple. The simplified block diagram of the converter is shown in Fig (2.1) Using a modified control scheme in the rectifier and inverter, the dc- link currents i_{dc1} & i_{dc2} are synchronised. This would result in reduced ripple in the dc-link capacitor. This solution is especially applicable when there is a specific relationship in the operating frequency between the two converters connected to the dc link.

In [13], this objective is achieved by using an active ripple reduction circuit in parallel to the capacitor as shown in Fig. (2.2).

The parallel leg added to the rectifier is essentially a bidirectional buck-boost

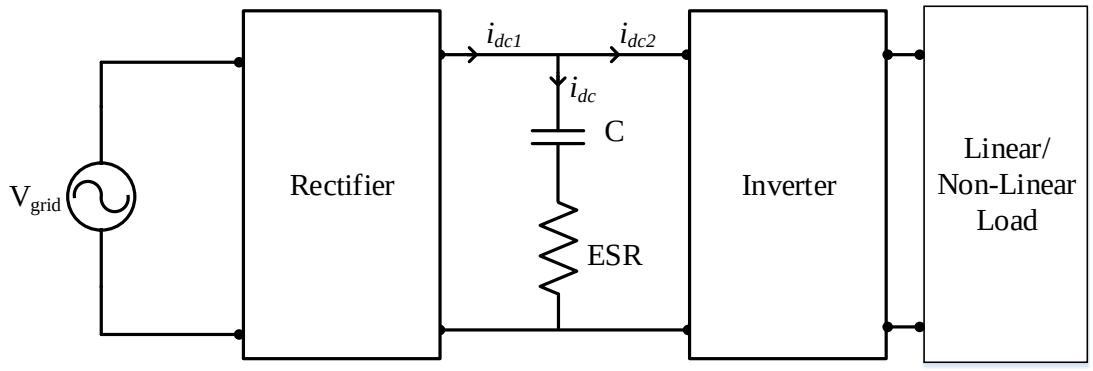

Figure 2.1: Additional control scheme for dc-link capacitance reduction

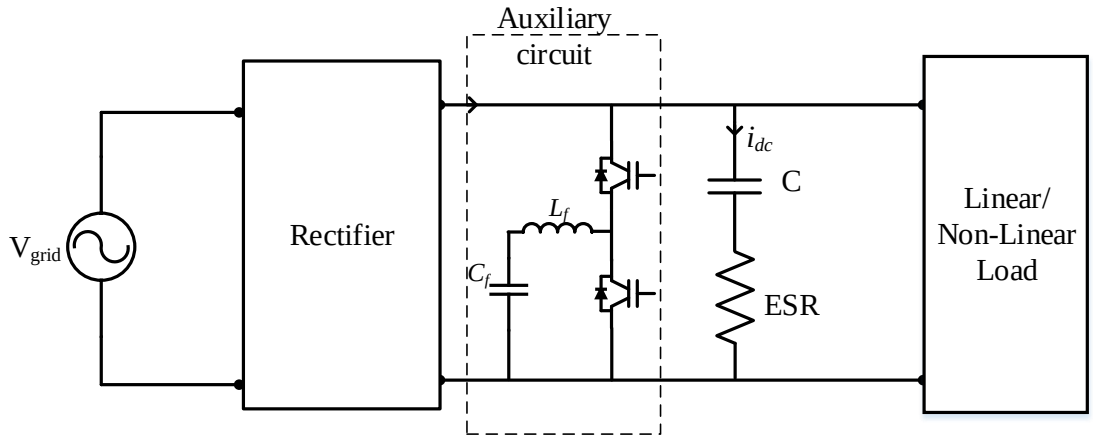

Figure 2.2: Parallel Connected Active Circuit

converter. The dc bus voltage is still controlled by the rectifier, while the ripple power that comes from the ac side is controlled by the auxiliary circuit. The switches are controlled to supply and draw power from the auxiliary capacitor C_f. The previously used capacitor in the dc-link is required to compensate only for the high frequency current ripple.

Apart from these methods, the dc-link capacitor can be replaced by an energy buffer as discussed in [14]. The energy buffer consists of a stacked switched capacitor bank made of film capacitors and can supply over 90% of the total stored energy in a cycle. This method, however, suffers from high voltage ripple in the dc-link and is costly.

2.2.2 Design of Capacitor banks

Though commonly used, there exists little systematic research into the design of capacitor banks. The traditional method of design involves choosing a combination of capacitors with sufficient rating to meet the terminal capacitance value at a specified voltage rating.

In [15], a novel approach is presented utilizing a hybrid capacitor bank. This capacitor bank would consist of both film capacitors and AECs. Both these capacitor families have different characteristics. Film capacitors have high current rating but low volume density and high cost per capacitance whereas AECs have relatively low current capability but low cost per capacitance and high volume density. This design leads to the film capacitor handling the high frequency current ripple in the dc-link. This corresponds to a reduction in the power dissipated in the AEC by virtue of the lower current stress and resulting in a longer lifetime.

Pelletier et al [16], discuss the optimisation of a DC-capacitor bank. The optimization is done with multiple constraints on the system such as capacitance value, rms current, voltage ripple and electromagnetic-compatibility (EMC).

A specific case is studied where the input filter of 1 kV buck converter is optimized. Optimization, with multiple constraints, is carried out for minimum volume and minimum surface area of the bank. However, optimization based on reliability is not considered. The current work carries out the reliability analysis of a capacitor bank made of AECs.

Chapter 3

Modelling of Aluminium Electrolytic Capacitor

3.1 Equivalent circuit of AEC

The equivalent circuit of an AEC based on the capacitor's material properties and geometry is shown in Figure 3.1Due to the physical design and construction, a capacitor not only has capacitance (C), but it also has an equivalent series resistance (ESR) and an equivalent series inductance (ESL).

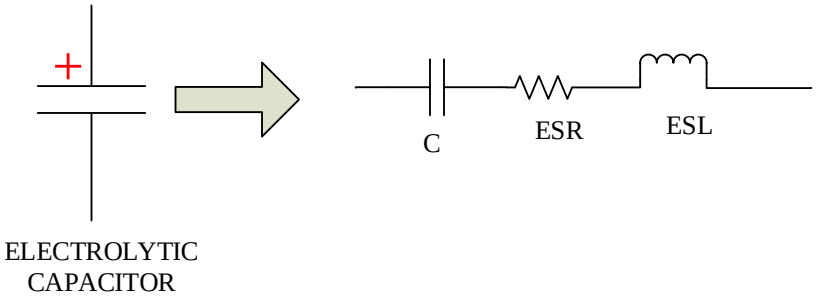

Figure 3.1: Equivalent Circuit diagram of AEC.

3.2 Modelling of parameters of AEC

3.2.1 Capacitance

The capacitance of AEC is expressed by,

$$C = \frac{\epsilon_o \epsilon_r A}{d} \tag{3.1}$$

where, ϵ_o= Dielectric constant in free space, ϵ_r=Relative dielectric constant of the dielectric (aluminium oxide), A= Surface area of the dielectric (in m^2), d = Thickness of the dielectric (in m)

The capacitance value varies with operating temperature and as well as the frequency of voltage applied to capacitor [17, 18]. The effective capacitance decreases as the frequency increases. For low frequency operation in capacitors capacitance value does not change [18]. For higher frequencies (greater than 10kHz), capacitance value become negligible.

3.2.2 Equivalent Series Resistance (ESR)

When AC ripple current flows through the capacitor, the presence of ESR leads to heat generation in the capacitor. ESR represents all of the ohmic losses of the capacitor and is modelled as a resistance in series with the capacitance C. The ESR of capacitor based on material properties and geometry can be expressed as,

$$ESR = \frac{d}{A_{cap}.\sigma_a} \tag{3.2}$$

where, A_{cap} is the surface area of the electrolytic capacitor, d is the average distance, σ_a is the conductivity of the electrolyte.

From (3.1,3.2) it can be seen clearly that the product of Capacitance and ESR, for any two capacitors made of the same materials, is constant. This assumption holds true, especially for a particular capacitor series.

When the capacitor is exposed to high temperature, the electrolyte of AEC would

expand. Due to increase in surface area of electrolyte, the resistance offered by it would decrease. Therefore, ESR declines with increasing in operating temperature [17].

3.2.3 Equivalent series inductance (ESL)

The ESL of a capacitor is a constant, and it is due to the capacitor terminal connection. The ESL of AECs varies from few nH to hundred of nHs [3]. Generally, this inductance does not affect the overall impedance at the switching frequencies of PECs (of the order of few tens of kiloHertz). Therefore, in case of PECs, it is possible to represent the AEC as series combination of ESR and capacitance, C

3.2.4 Temperature dependence of C & ESR

As has been mentioned before, the capacitance and ESR of an AEC are highly dependent on temperature. this dependence can be modelled from the material properties as follows [19, 20].

$$\varepsilon = \varepsilon^{(0)} \cdot e^{B/T} \tag{3.3}$$

$$\sigma = \sigma_A \cdot [1 + D \cdot (T - T_A)] \tag{3.4}$$

where $\varepsilon^{(0)}$ is base permittivity, σ_A is base conductivity at reference temperature T_A and B, D are constants specific to the chosen material.

Chapter 4

Proposed scheme for reliability analysis

To assess the reliability of any electronic system, the predominant method was to use handbook based calculations (MIL-HDK-217F, 338B)[21, 22]. In recent years this trend has shifted to incorporate Physics-of-Failure (PoF) based methods for the same analysis. PoF based methods require knowledge of the failure processes (physical/chemical) along with their dependence on system parameters and external factors. These methods are superior as they allow us to integrate the mission-profile of the system and perform statistical analysis. [23]

Existing analysis on reliability assumes that the operating conditions of the capacitor are constant throughout the life of the device. The current work uses a dynamic simulation study to incorporate the changes in operating conditions of the capacitor. The method consists of an iterative process of circuit simulations followed by thermal simulations. The circuit simulations require the physical parameters of individual components such as capacitance, Irradiation, ambient temperature, etc. The values of these physical parameters are in turn dependent on the power dissipation derived from the previous circuit and thermal simulations. Also, the degradation parameters vary with temperature. To account for all these effects, the lifetime of the system is implemented by incremental time steps where the parameters are

updated in each step.

4.1 Bank stress reduction

Consider a dc-link capacitor bank which consists of n number of strings and m capacitors in each string (m**x**n bank). All capacitors in the bank are of the same rating. Let C_{ind} be the capacitance and R_{ind} be the ESR of each individual capacitor in the bank. As mentioned before, for a given series of capacitors, it follows that the product of capacitance and ESR is constant. Now capacitance and ESR of each string with m capacitors in series is,

$$C_{str} = \frac{C_{ind}}{m} \tag{4.1}$$

$$R_{str} = R_{ind} * m \tag{4.2}$$

where, C_{str} and R_{str} is the capacitance and ESR of the string respectively.

Then the total capacitance C_{to} and ESR, R_{to} of the mXn bank can be given by,

$$C_{to} = \frac{C_{ind} * n}{m} \tag{4.3}$$

$$R_{to} = \frac{R_{ind} * m}{n} \tag{4.4}$$

As the capacitor bank is designed to meet a certain terminal capacitance value, the total current flowing through the capacitor bank is fixed at I_{to}. Then the current through each string can be given by,

$$I_{str} = \frac{I_{to}}{n} \tag{4.5}$$

The thermal power loss in each capacitor is given by,

$$P_{ind} = I_{str}^2 * R_{ind} \tag{4.6}$$

Substituting 4.2,4.4 and 4.5 in 4.6 we get,

$$P_{ind} = \frac{I_t^2.R_t}{m * n} \tag{4.7}$$

It is seen that for a given value of terminal capacitance, the stress on individual capacitors decreases with increase in the size of the capacitor bank.

4.2 Algorithm to find time to failure of the capacitor bank

Flowchart shown in Fig.4.1 is used to find the time to failure of the capacitor bank. Prior to the start of the system, the physical parameters (C & ESR) and base degradation rates are initialized. With these initial values, the inverter is simulated to find the steady state value of rms current in each capacitor. The rms current is then used to calculate the core temperature by the thermal model specified in Section 4.3 Using the core temperature, the degradation rates and values of C & ESR are calculated at that temperature. With the obtained values of C & ESR, each capacitor in the bank is checked for soft failure. If the capacitor bank is healthy, these updated parameter values are used and the simulation is run again. The increment in time for each iteration considered is chosen at 10 hrs per step. This iteration is done until at least one capacitor in the bank reaches its end-of-life. The end-of-life is defined as the time at which either the capacitance reduces by 20% or the equivalent series resistance increases by 200% [24]. The number of time steps taken to reach the failure state is used to find the Time to Failure.

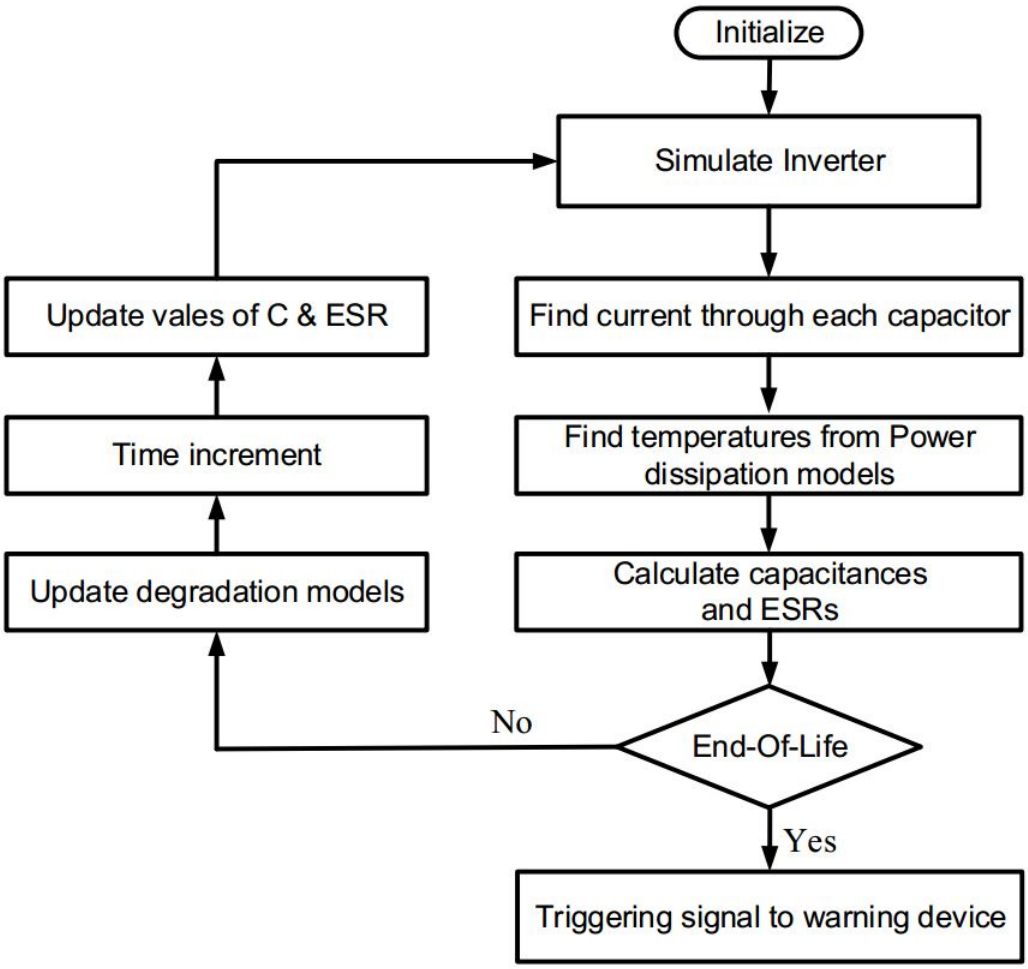

Figure 4.1: Flowchart of system operation

4.3 Power dissipation and degradation modelling of AEC

The prominent degradation mechanism of AECs is the evaporation of the electrolyte. The rate of evaporation of the electrolyte and by extension, the degradation rate of the capacitor is dependent on the core temperature of the AEC. Different load conditions lead to variation in current through the capacitor and also in the core temperature. It is imperative that the core temperature must be estimated to accurately monitor the rate of degradation. The heat transfer that occurs in an AEC consists of two parts. The first part transfers heat from the core of the capacitor to the case via conduction, axially and radially. The second part involves transfer from the case to the surroundings consisting of both radiation and free convection.

The temperature distribution in the bank can be calculated using multiple methods such as Finite Element Analysis (FEA) and mathematical simulations [25]. Though these complex methods can be used for estimating the temperature rise due to the mentioned modes of heat transfer, the simple model shown in Fig.4.2 is sufficient for our purpose [26].

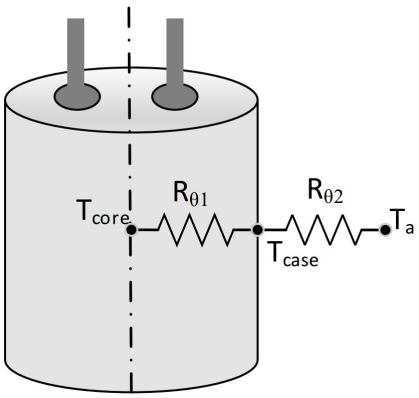

Figure 4.2: Thermal Model of Capacitor

The thermal power loss $P(t)$ in the capacitor at time t and core temperature T is given by

$$P(t) = I^2_{c_{rms}}(t).ESR(T,t) \tag{4.8}$$

where $I_{c_{rms}}(t)$ is the root mean square value of current is passing through it and $ESR(T,t)$ is the ESR of the capacitor at a given time t and temperature T. Using this value of dissipated power, the core temperature can be found by the following equation.

$$T = T_a + P(t).(R_{\theta 1} + R_{\theta 2}) \tag{4.9}$$

where, T_a is the ambient temperature, $R_{\theta 1}$ models the heat transfer by conduction from the core to the case and $R_{\theta 2}$ corresponds to the heat transfer via convection and radiation.

The degradation of AEC is a function of time, temperature and frequency. For a given application, the frequency content is assumed to be constant. At a fixed load if the temperature is considered to be constant then C decreases linearly and the

ESR increases exponentially as function of time [27]. This is modelled as:

$$CAP\,(t) = CAP_o\,(1 + A.t) \tag{4.10}$$

$$ESR\,(t) = ESR_o e^{C.t} \tag{4.11}$$

where, CAP_o and ESR_o are the initial values of capacitance and ESR of the capacitor. The constants A and C in the equation are temperature dependent degradation rates and are assumed to follow the Arrhenius equation which gives the temperature dependence of reaction rates.

$$A\,(t) = A_o.e^{-X/T} \tag{4.12}$$

$$C\,(t) = C_o.e^{-Y/T} \tag{4.13}$$

where, Ao and Bo are base degradation rates. X and Y are constants for a particular capacitor. In (4.10) the temperature dependence of CAP_o and ESR_o can be incorporated using the material properties and basic equations (3.1,3.2) as:

$$CAP_o = \varepsilon_o.\varepsilon^{(o)}.e^{B/T}.\frac{A_{cap}}{d} \tag{4.14}$$

$$ESR_o = \frac{d}{A_{cap}.\sigma_A\,[1 + D\,(T - T_A)]} \tag{4.15}$$

where, A_{cap} is the surface area of the electrolytic capacitor, ε_o is the absolute permittivity and ε^0 is base permittivity, d is the average distance between electrodes, σ_A is the base conductivity, T_A the reference temperature.

To take into account the temperature changes as a function of time, the values of capacitance and ESR have been calculated incrementally. The accumulated value of these parameters at any time t_a and instantaneous temperature $T(t_a)$ derived using (4.10) and (4.11) is (see Appendix A) At any instant t_a and instantaneous $T(t_a)$ is

given by:

$$CAP\left[T\left(t\right),t_a\right] = CAP'.e^{\frac{B}{T(t_a)}}\left\{1+\int_0^{t_a} A\left[T\left(t\right)\right]\right\}dt \tag{4.16}$$

$$ESR\left[T\left(t\right),t_a\right] = \frac{ESR'}{1+D\left[T\left(t\right)-T_a\right]}.e^{\int_0^{t_a} C[T(t)]dt} \tag{4.17}$$

where

$$CAP' = \varepsilon_o.\varepsilon^{(o)}.\frac{A_{cap}}{d} \tag{4.18}$$

$$ESR' = \frac{d}{A_{cap}.\sigma_A} \tag{4.19}$$

The values of CAP', A_o, B for capacitance and ESR_o, C_o, D for ESR' are determined using the capacitor data sheet [3]. For a given capacitor series, the degradation constants are the same irrespective of the value of capacitance.

4.4 Monte Carlo Simulations

As the models used, circuit, thermal and degradation, are deterministic, the value of time to failure obtained is a fixed value. However, practical systems are subject to variations in the physical parameters of individual components. For example, in the present system, the variation in the value of capacitance of AEC is considerable. Datasheets of commercially available AECs report a tolerance in the value of capacitance as +/- 20%. To incorporate for these variations, the standard method is to use Monte Carlo (MC) simulations. The MC simulations would calculate the distribution of the predicted time to failure and thereby exclude outliers. This method consists of running the simulation iteratively with a set of inputs as random variables followed by an examination of the outputs [28]. In the present study, the values of capacitance and ESR are sampled from a normal distribution and circuit

is simulated with these values and Mean Time to Failure (MTTF) are reported. As this analysis is computationally intensive, it is performed for the following configurations, single capacitor, 1**x**2, 2**x**2. These configurations are also verified on a hardware setup.

4.5 Simulation Results and discussion

A single phase grid connected solar inverter as shown in Fig.(4.3) is used as the base

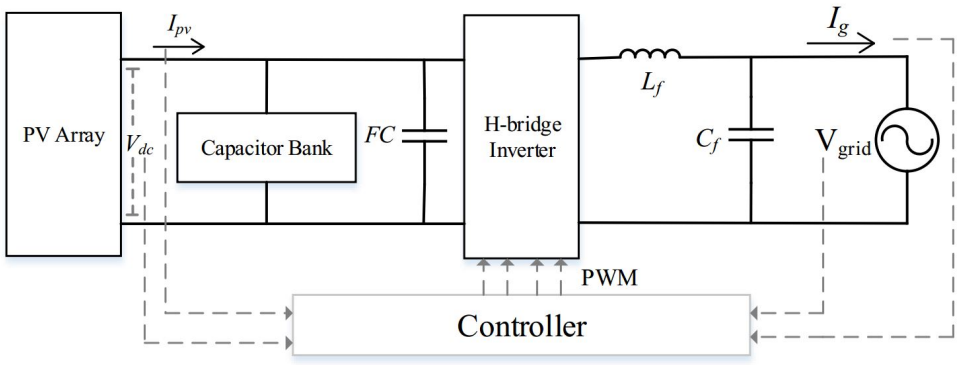

Figure 4.3: Generic single phase grid connected PV system used for simulation

application to test the reliability of the capacitor bank. Simulations are performed on MATLAB-Simulink platform. The inverter specifications are listed in Table 4.1. For operation in the grid-feeding mode, the inverter consists of two control loops, an outer voltage control loop and inner current control loop. The dc-link voltage reference is chosen manually at the Maximum Operating Point(MPP) of the PV Panels. The waveforms of grid current, voltage and Inverter output voltage are shown in Figure 4.4

Capacitor banks of different configurations are simulated. It is ensured that the terminal value of the capacitance is maintained close to the design requirements. The degradation parameters are estimated from the datasheet of the capacitors used. To ensure that no outliers are encountered, the capacitance value of the individual AECs are sampled from a normal distribution as discussed in section 4.4. Three such values are chosen and the MTTF is reported. The MTTF for each of these

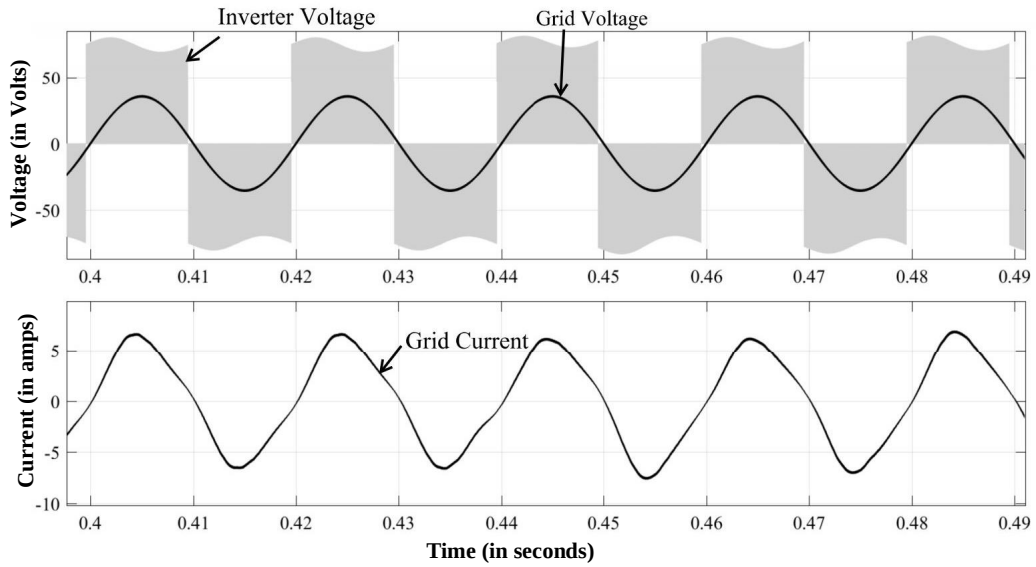

Figure 4.4: Waveforms of simulated inverter

Table 4.1: Inverter Specifications

Parameter	Variable	Value
Maximum Power	P_{MPP}	112.5 W
Voltage at Pmax	V_{MPP}	75 V
Current at Pmax	I_{MPP}	1.5 A
Short circuit current	I_{SC}	2.1 A
Open circuit voltage	V_{OC}	100 V
Terminal Capacitance	C_t	560 μF
Terminal ESR	R_t	180$m\Omega$

banks is shown in Fig. 4.5

It is seen that the reliability of bank increases as the size of the bank increases. The size of a capacitor bank is defined here as the product of parallel strings (n) and the number of series capacitors in a string (m).

It is expected that among two banks of the same size and different configurations, the bank with more number of parallel strings would have a higher life, e.g., between a 1**x**2 and 2**x**1 bank, the 1**x**2 bank shall be more reliable. The justification for this is derived from basic circuit laws. Assume at that a given instant for two capacitors connected in parallel, capacitor C1 has a lower capacitance value than capacitor C2. In an application with low-frequency current ripple, C2 shall have a higher current

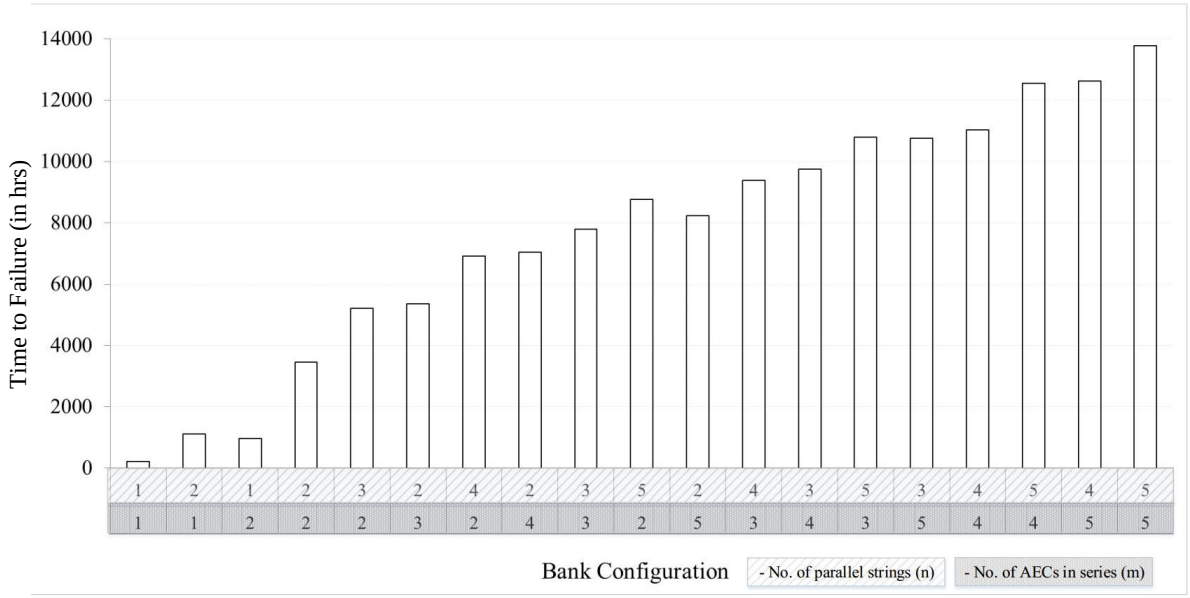

Figure 4.5: MTTF for various banks

flowing through it. This would lead to a faster degradation in C2 as compared to C1. With the passage of time, the difference in the values of C2 and C1 would decrease and then eventually both the capacitors degrade at the same rate. This balancing effect shall ensure that the stress is evenly distributed among the multiple capacitor strings and thereby increase the reliability of the entire bank. Similar reasoning exists for high-frequency applications where the balancing action is done by ESR rather than the capacitance.

However, it is found in simulations that this effect is quite negligible as compared to the effect of increasing the size of the bank.

For validation of the observed phenomenon on hardware, three capacitor bank configurations, single capacitor, 1**x**2, 2**x**2 are chosen. For these configurations, Monte Carlo simulations to find time to failure is run. These simulations assume that individual capacitances follow a normal distribution ($\mu = 504\mu F, \sigma = 37\mu F$). 300 such values of capacitance for each capacitor bank are randomly sampled from this distribution and used in the inverter model. For each set of capacitance values, the time to failure is estimated and recorded. Figures 4.6 to 4.8 and Table 4.2 summarise the findings of these simulations. From Table 4.2, it is seen that the MTTF

of the capacitor bank increases as the size of the capacitor bank increases.

Table 4.2: TTF distribution

Bank Configuration	MTTF (in hrs)	Variance
Single Capacitor	207	26
$1X2$	1082	64
$2X2$	3466	223

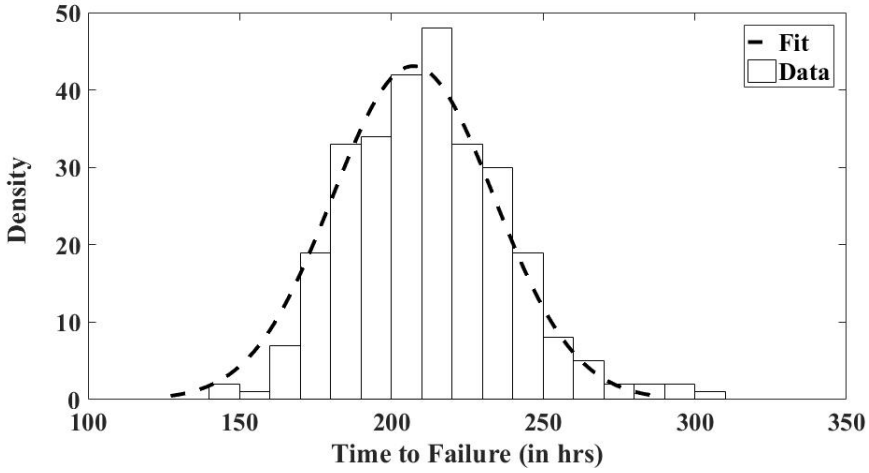

Figure 4.6: TTF for Single Capacitor

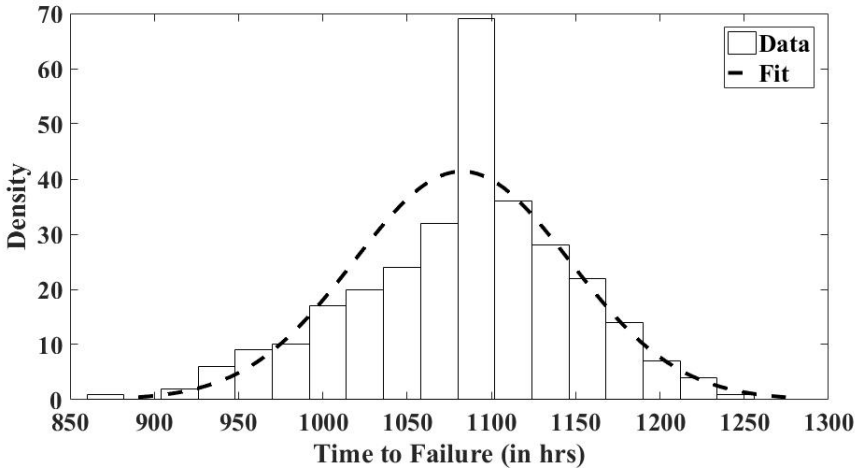

Figure 4.7: TTF for $1X2$ bank

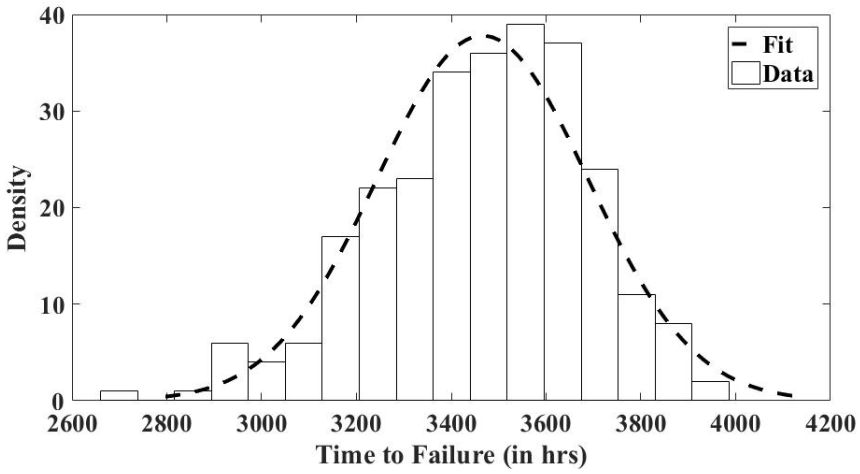

Figure 4.8: TTF for $2X2$ bank

4.6 Accelerated Life Testing of Capacitor

To test the proposed method in a limited time frame, accelerated life testing (ALT) methods are used. Two methods for ALT of capacitors consist are discussed in literature [29, 30, 31, 32]. In [29], current ripple is injected into the capacitor to perform ageing. Two factors, ambient temperature and ripple current characteristics (continuous or intermittent) are changed and life of the capacitor is compared. In [31], the capacitor is operated at an ambient temperature higher than the rated value. This is also known as Thermal Overstress (TOS) ageing. The method discussed in [32] proposes accelerated ageing of capacitors by puncturing the top seal of the capacitor. As discussed in Section 4.3, the predominant process of degradation is evaporation of electrolyte. By puncturing the top seal of the capacitor, this rate of evaporation can be increased. For even faster degradation, the capacitor can be operated at a higher ambient temperature.

Chapter 5

Experimental Results

5.1 Laboratory prototype

To validate the proposed reliability analysis of dc-link capacitor banks, an experimental prototype of single phase grid connected PV inverter is built. The inverter and PV module parameters are specified in Table 5.1

Table 5.1: Inverter Parameters of experimental setup

Parameter	Value
PV Open circuit Voltage	$V_{oc} = 100$V
PV Short Circuit Current	$I_{sc} = 2.1$A
PV Voltage at MPP	$V_{MPP} = 75$V
PV Current at MPP	$I_{MPP} = 1.5$A
Inductor	$L = 3.1mH$ and $R = 0.2\Omega$ at 100Hz
Grid frequency	$f_o = 50Hz$
Grid Voltage	$V_{grid} = 25V_{rms}$
Switching Frequency	$f_s = 10kHz$

System parts and their attributes are tabulated in Table 5.2.

The inverter switches are realised using an IGBT module (FSBB20CH60C), which includes integrated short circuit protection and in-built gate drivers. PV array is emulated using Agilent Technologies made E4360A Solar Array Simulator. DSP (Digital Signal Processor) TMS320F2808 is used for the closed loop control. PWM signals for IGBT's are generated using interrupt-based timer modules of the

Table 5.2: Components used in experimentation

Part	Attribute
Solar Array Simulator	E4360A (1200W) (Agilent Technology)
DSP Kit	TMS320F2808 (32-Bit with flash) (Texas Instruments)
IGBT Module	FSBB20CH60C (600V, 20A 3-phase IGBT inverter) (with integrated gate drivers and SC protection)
Current Sensor	LA-25P (55A) (LEM)
Op-amp	LF353 (JFET-Input) (Texas Instruments)
ICs	74HCT240(Inverting IC) LM317 (for 1.5V offset)
Diode Zener Diode	IN4007 BZT52C3V3-E3-08(3.3V, .5 W) (Vishay Semiconductors)
Variac	1-pahse, 15A (Dimmerstat)
Linear Power Supply	Transformer (230/18) ICs 7815 and 7819 W04 Bridge rectifier Capacitor (470μF)

controller. As the actual feedback signals are at a higher level than supported by the controller's ADC, they are attenuated using OP-AMP based differential amplifier circuits. Inductor and PV currents are measured using LEM-LA-25P current transducers. The op-amps and transducers are connected on a sensing board. The OP-AMPS, transducers, IGBT driver circuit and other ICs are powered using a regulated $\pm$15V supply generated from a linear power supply circuit. The complete experimental setup is shown in Fig. (5.1)

1) Sensing Board

The sensing board acts as an interface between the power circuit and the DSP. The input taken by the DSP (for ADC) and output given (as PWM) are unipolar voltage signals between 0V and 3.3V. Also, the DSP has limited current soucing

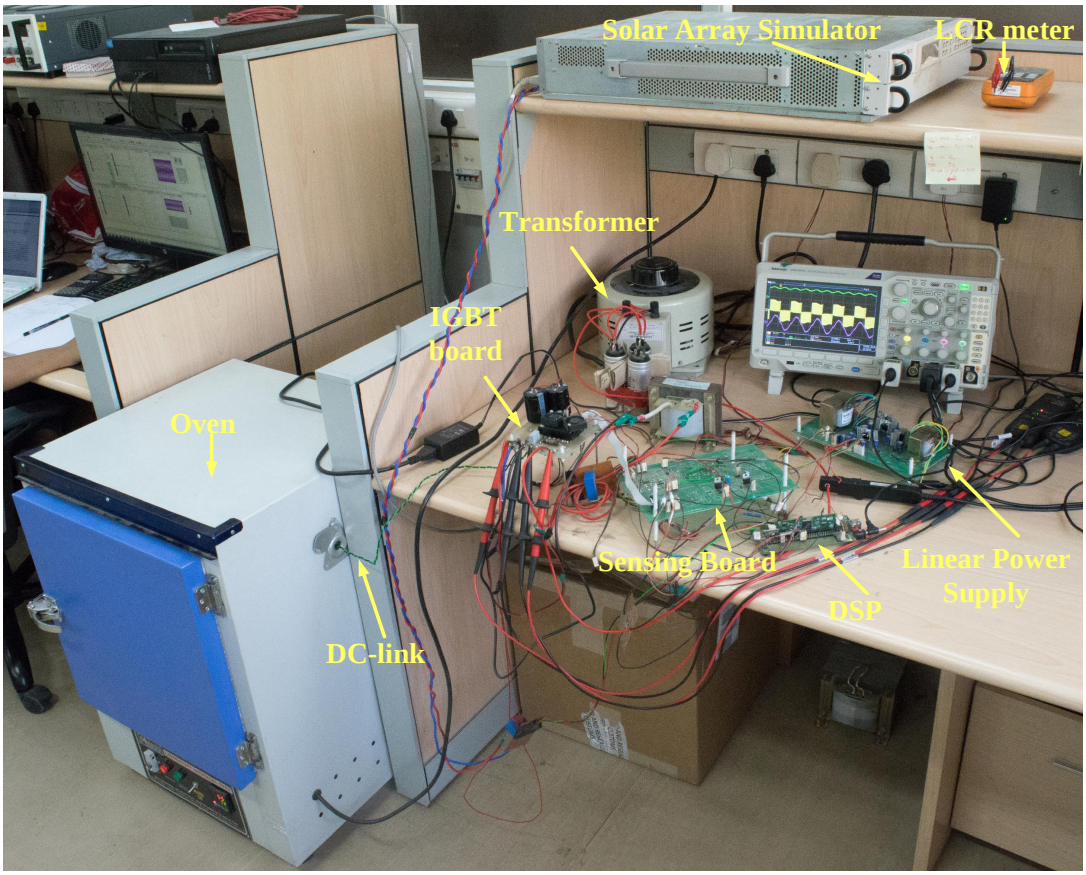

Figure 5.1: Experimental Setup

capability. These shortcomings are taken care by the sensing board. The power supply for the ICs is provided by an external Linear Power Supply (LPS). The AC signals are attenuated and combined with a 1.5V dc supply to make sure that the DSP inputs remain within the specified values.

2) Digital Signal processor (DSP)

The DSP, TMS320F2808 is used for the system control . Two modules, ADC and PWM, of the DSP are used for our purpose. The sensed signals which are grid, dc-link, offset voltages and grid, PV current are given as inputs to the ADC Module. The sampling frequency of ADC is set at 100μs. The offset of 1.5V is subtracted from the sensed grid voltage and sensed currents. The sensed grid voltage and current are used to for PLL operation and to ensure UPF operation of the inverter. Dc-link voltage and grid current are utilised for closed loop control and obtain PWM signals. Unipolar Sine-triangle PWM is used for operation of the inverter.

3) Power Inverter and Drivers

The H-bride inverter is made utilising the two legs of FSBB20CH60C (IGBT module) as shown in Fig.(5.2). Each IGBT is rated for 600V and 20A. It has

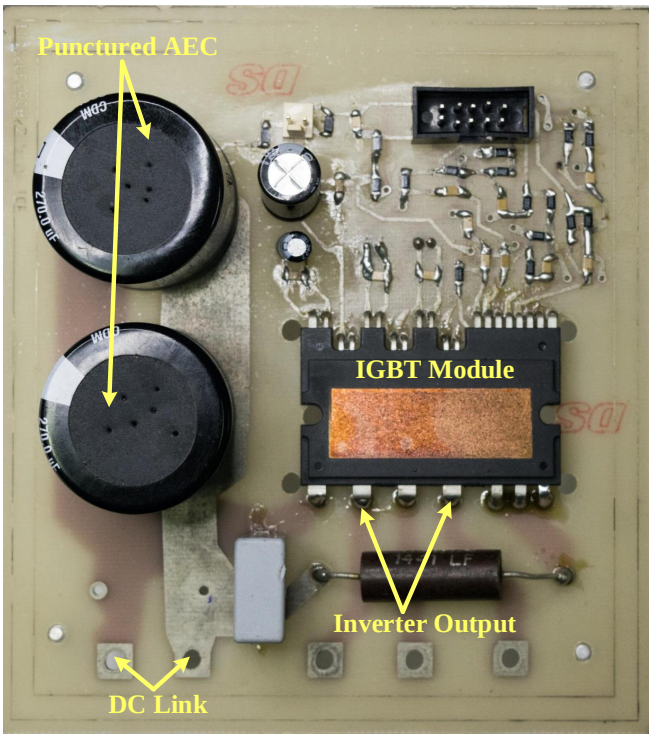

Figure 5.2: Inverter Board

integrated short circuit protection and inbuilt gate drivers. The solar array simulator is connected to IGBT module via DC-link AEC capacitor bank. The PWM signals from DSP are fed to the module. The dc-link voltage and PV current are feedback to the DSP for closed loop control via sensing board.

4) Oven

As mentioned in Section 4.6, the capacitor bank is degraded using accelerated ageing techniques as discussed in 4.6. The capacitors are punctured and placed in an oven operating at higher temperature. The setup to achieve this is shown in Figs.(5.3,5.4)

The capacitor bank is then connected to the dc-link of the inverter using a low inductance twisted wire. To avoid any effect due to the high frequency ripple in the dc-link, a 10 μF film capacitor is connected in parallel with the bank.

Figure 5.3: Top view of Punctured Capacitor

5.2 Experimental results of proposed method

The prototype is run in grid feeding mode at UPF with parameters as mentioned in Table 5.1.Waveforms of grid current, dc-link voltage and inverter output voltage are shown in Fig.(5.5) The inverter setup is run for three bank configurations single capacitor, 1**x**2, 2**x**2. For each of these configurations, the prototype is operated and the values of C & ESR of individual capacitor is monitored timely using a LCR meter (Keysight U1733C). The experiment is performed for a duration of 100 hrs for each capacitor bank configuration.

It is found that the decrease in capacitance for the entire operation of the inverter is negligible compared to the change in the ESR. Therefore the percentage increase of ESR is used as the indicator of degradation of the capacitor. The results are shown in Figures 5.6 to 5.8

The highest value of degradation in any capacitor is reported in Table 5.3

Table 5.3: Comparison of degradation

Bank Configuration	Maximum increase in ESR (in %)
Single Capacitor	30.1%
$1X2$	12.7%
$2X2$	3.52%

From the data it is inferred that the 2**x**2 capacitor bank has degraded the least and the singe capacitor has degraded the most.

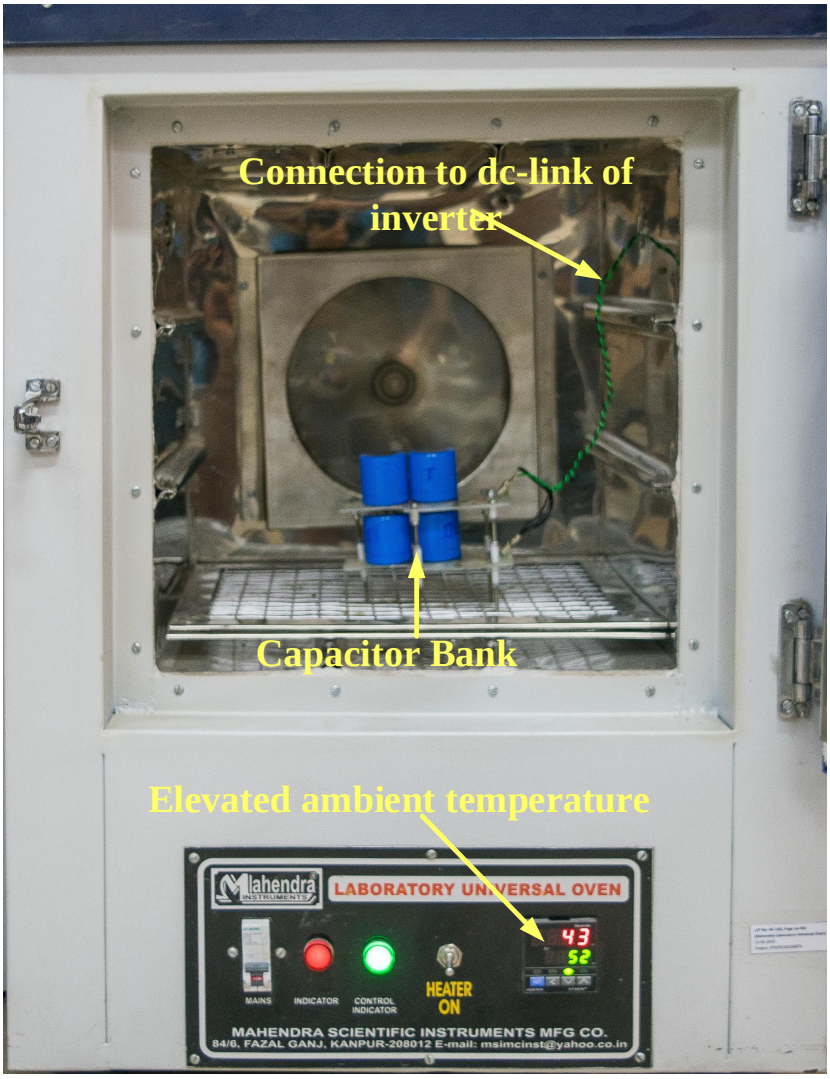

Figure 5.4: Setup for accelerated ageing of capacitor bank

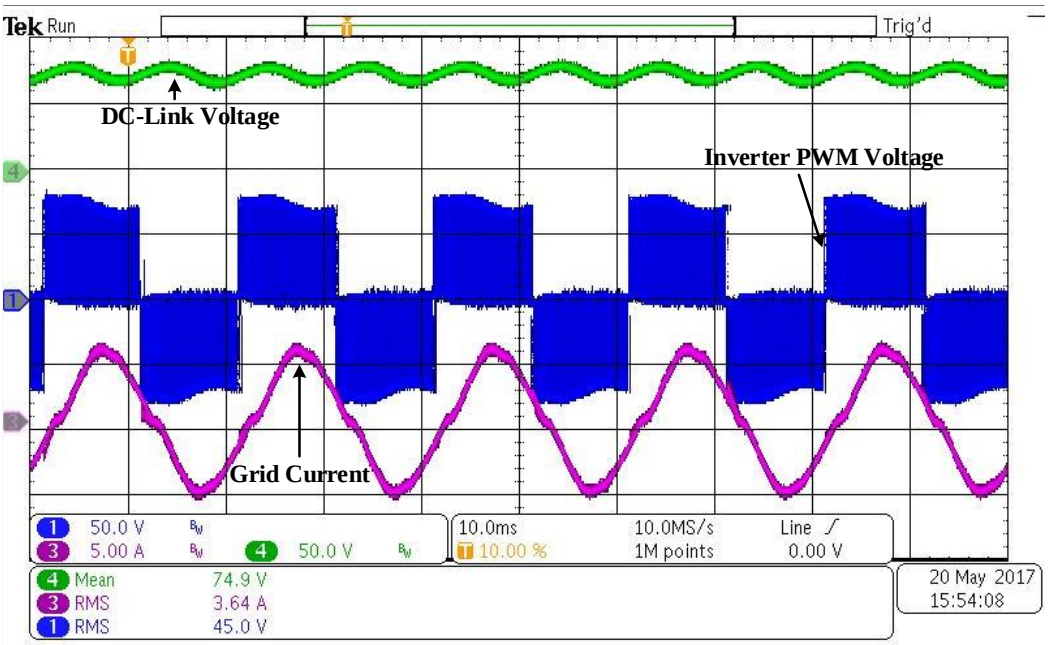

Figure 5.5: Waveforms of Grid Current(Pink : 5A/div), Inverter PWM Voltage(Blue : 50V/div), DC-link Voltage(Green : 50V/div)

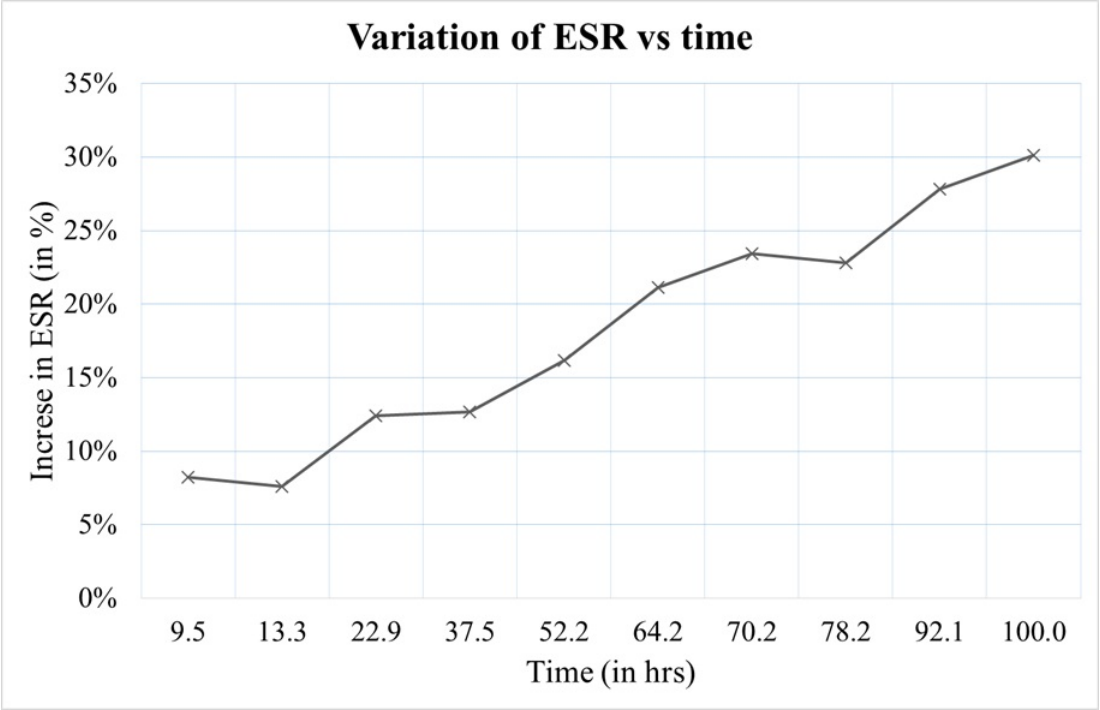

Figure 5.6: Variation in ageing of single capacitor

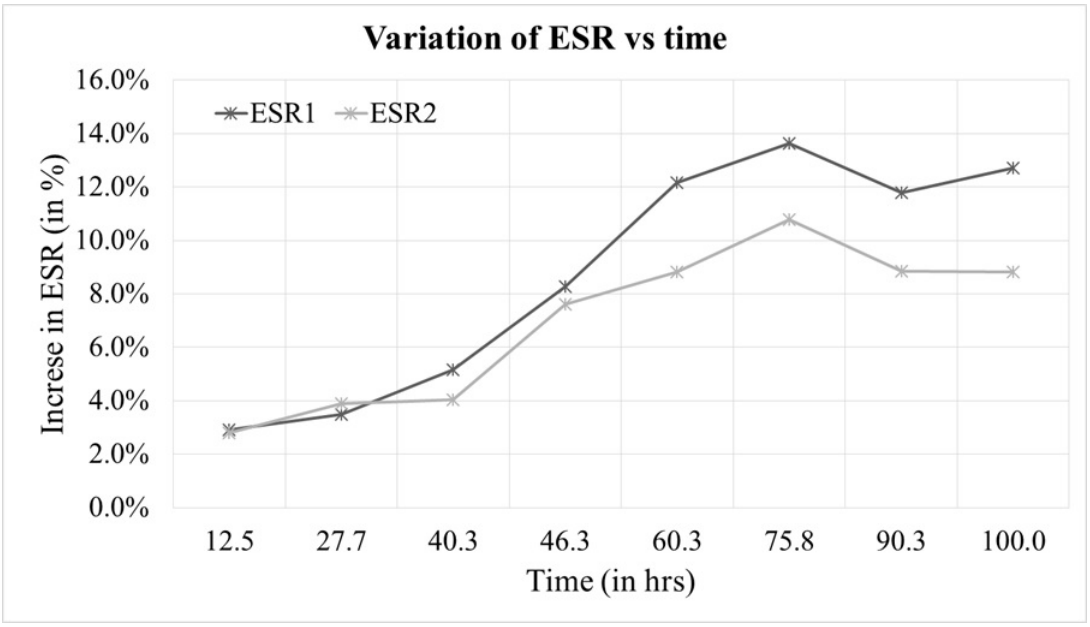

Figure 5.7: Variation in ageing of 1x2 capacitor bank

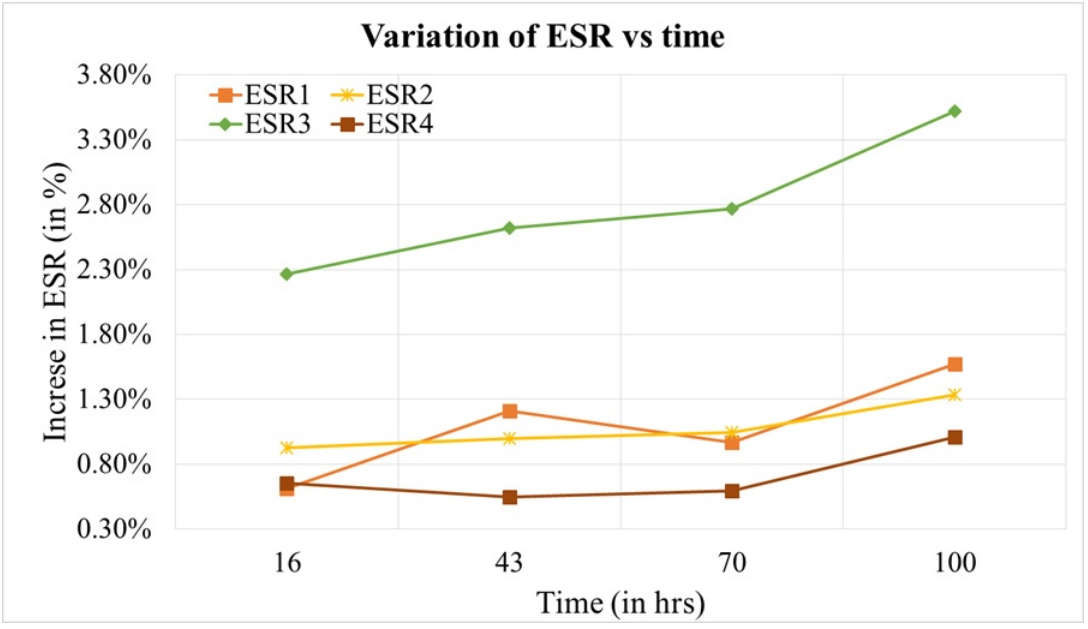

Figure 5.8: Variation in ageing of 2x2 capacitor bank

Chapter 6

Conclusions and future works

6.1 Conclusions

The main purpose of this thesis is reliability analysis of a dc-link capacitor bank. A Physics-of-Failure based methodology is used to find the Time to failure of the different capacitor bank configurations. The following are the key findings:

1. For a given value of terminal capacitance, it is beneficial from a reliability point of view to increase the size of the capacitor bank. This claim is checked by simulations and is verified by experimentation

2. When the size of the capacitor bank is fixed, the distribution between number of capacitors in series and number of parallel strings has negligible affect on the reliability of the entire capacitor bank.

6.2 Scope for future work

6.2.1 Incorporation of mission profile into reliability analysis of system

In a practical inverter, the load and ambient temperature are subject to variations with time. These variations may have significant effect on the reliability of the capacitor bank and have to be studied.

6.2.2 Condition monitoring of individual capacitors in banks

Existing literature on condition monitoring is aimed at finding the equivalent C & ESR of the dc-link capacitor bank. However, soft failure of any single capacitor in the bank increases the chance of catastrophic failure. This leads to open-circuiting of the capacitor and would affect the entire operation of the inverter. It is therefore imperative to find online methods for condition monitoring of individual capacitors in the bank.

Appendix A

Derivations

With time, as the AEC degrades, capacitance decreases and ESR increases [27, 17]. For operation at constant temperature and fixed frequency spectrum, this variation can be modelled as

$$CAP\,(t) = CAP_o\,(1 + A.t) \tag{A.1}$$

$$ESR\,(t) = ESR_o e^{C.t} \tag{A.2}$$

As in most practical cases, the operating temperature is a function of time. This effect can be incorporated into Equations (A.1) and (A.2) by changing the CAP and ESR values incrementally. In a period Δt, the increment is given by

$$\Delta \frac{\mathrm{CAP}[T(t), t]}{\mathrm{CAP}_T} = A[T(t)] \cdot \Delta t \tag{A.3}$$

$$\ln \Delta \frac{\mathrm{ESR}[T(t), t]}{\mathrm{ESR}_T} = C[T(t)] \cdot \Delta t \tag{A.4}$$

Summing up the increments for n time steps,

$$\frac{\mathrm{CAP}[T(t),n]}{\mathrm{CAP}_T} = \sum_0^n \Delta \frac{\mathrm{CAP}[T(t),t]}{\mathrm{CAP}_T}$$
$$= \sum_0^n A[T(t)] \cdot \Delta t \tag{A.5}$$

$$\frac{\mathrm{ESR}[T(t),n]}{\mathrm{ESR}_T} = \sum_0^n \Delta \frac{\mathrm{ESR}[T(t),t]}{\mathrm{ESR}_T}$$
$$= \ln \prod_0^n \Delta \frac{\mathrm{ESR}[T(t),t]}{\mathrm{ESR}_T} \tag{A.6}$$

These equations written in the integral form gives

$$\frac{\mathrm{CAP}[T(t),x]}{\mathrm{CAP}_T} = \int_0^n A[T(t)] \cdot dt + E \tag{A.7}$$

$$\frac{\mathrm{ESR}[T(t),n]}{\mathrm{ESR}_T} = e^{\int_0^n C[T(t)] \cdot dt + D} \tag{A.8}$$

The boundary conditions for this integral are

$$\mathrm{CAP}[T(0),0] = \mathrm{CAP}_T \tag{A.9}$$

$$\mathrm{ESR}[T(0),0] = \mathrm{ESR}_T \tag{A.10}$$

Solving and substituting in Equations (A.7) and (A.8) gives

$$\frac{\mathrm{CAP}[T(t),x]}{\mathrm{CAP}_T} = \int_0^n A[T(t)] \cdot dt + 1 \tag{A.11}$$

$$\frac{\mathrm{ESR}[T(t),n]}{\mathrm{ESR}_T} = e^{\int_0^n C[T(t)] \cdot dt} \tag{A.12}$$

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